Three-dimensional optoelectronic stacked processor by use of free-space optical interconnection and three-dimensional VLSI chip stacks

Guoqiang Li, Dawei Huang, Emel Yuceturk, Philippe J. Marchand, Sadik C. Esener, Volkan H. Ozguz, and Yue Liu

We present a demonstration system under the three-dimensional (3D) optoelectronic stacked processor consortium. The processor combines the advantages of optics in global, high-density, high-speed parallel interconnections with the density and computational power of 3D chip stacks. In particular, a compact and scalable optoelectronic switching system with a high bandwidth is designed. The system consists of three silicon chip stacks, each integrated with a single vertical-cavity-surface-emitting-laser–metal-semiconductor-metal detector array and an optical interconnection module. Any input signal at one end stack can be switched through the central crossbar stack to any output channel on the opposite end stack. The crossbar bandwidth is designed to be 256 Gb/s. For the free-space optical interconnection, a novel folded hybrid micro–macro optical system with a concave reflection mirror has been designed. The optics module can provide a high resolution, a large field of view, a high link efficiency, and low optical cross talk. It is also symmetric and modular. Off-the-shelf macro-optical components are used. The concave reflection mirror can significantly improve the image quality and tolerate a large misalignment of the optical components, and it can also compensate for the lateral shift of the chip stacks. Scaling of the macrolens can be used to adjust the interconnection length between the chip stacks or make the system more compact. The components are easy to align, and only passive alignment is required. Optics and electronics are separated until the final assembly step, and the optomechanic module can be removed and replaced. By use of 3D chip stacks, commercially available optical components, and simple passive packaging techniques, it is possible to achieve a high-performance optoelectronic switching system. © 2002 Optical Society of America

OCIS codes: 200.0200; 200.4650; 200.4960; 200.2610.

1. Introduction

With the rapid development of VLSI technology, integration density, chip area, and processor clock speed have been increasing continuously. To efficiently exploit the performance of microelectronic cir-
terconnection technologies must be developed as alternative solutions of long-term potential.

Optical interconnection has been widely accepted as a promising approach for massively parallel data communications. In comparison with their electronic counterparts, optical links have low cross talk and low sensitivity to electromagnetic interference. With a 2D array of optoelectronic transmitters and receivers, high-density (several thousands of channels/cm²) and high-data-rate (Gb/s) interconnections can be achieved with a high bandwidth of several Tb/s/cm². The surface-emitting characteristic of the vertical-cavity surface-emitting lasers (VCSELs) allows the optoelectronic chip to be integrated onto the top of the silicon chip so that the third spatial dimension can be used for beam routing. Therefore three-dimensional (3D) optical interconnects permit a high utility of the chip area, and the number of interconnection channels can scale with the chip area. For two fixed optoelectronic arrays, different links have almost the same optical path length, and hence optical interconnects have less signal skew. In the past few years, various demonstration systems have been reported, especially at multiple-chip-module and board levels. The beam propagation medium can be free-space optics, fiber optics, or optical waveguides. Significant progress has been made in optoelectronic devices, integration of optoelectronic devices with complementary-metal-oxide-semiconductor circuits, micro-optics fabrication, and system packaging on the basis of optomechanics, planar, or stacked integration.

In parallel, advances in 3D VLSI packaging technologies have made it possible to integrate multiple chips into a smaller volume by stacking electronic chip dies on top of each other. Three-dimensional chip stacks can realize more powerful processing functions than planar architectures and significantly reduce power consumption and latency by shortening the length of interconnections between one chip and its neighbors. However, this approach cannot support the density and globality of electrical interconnects that are required by many operations when the overall system contains several stacks, each containing many chips. In this case, free-space optics can provide a much needed global, high-speed, high-density communication capability between stacks.

Higher-level digital signal-processing systems require densely distributed nodes (processing elements) with larger complexity and global connectivity. By combining the strengths of 3D chip packaging and optoelectronic parallel array interconnection technologies, it is possible to build an efficient compact system that permits fast processing and switching of large data arrays. The powerful nodes are integrated into the 3D chip stacks with each chip containing an array of processing elements or other complex circuits. Such a system can be utilized for implementation of various applications including digital image processing, fast Fourier transform, and bit-parallel crossbar switch. In particular, one can construct a system composed of several processor stacks that are optically interconnected with a crossbar stack. An all-electronic implementation of the crossbar network has difficulty in scalability and thus has a limited bandwidth. In this paper we describe the realization of a 3D optoelectronic stacked processor system with a focus on the crossbar switch that is scalable and has a high bandwidth. The system consists of three layers: electronics, optoelectronics, and optics. The electronic layer has three silicon chip stacks with each stack comprising 16 VLSI chips. Each chip corresponds to 16 optical inputs–outputs (I/Os) and realizes 16 × 16 switches at 1 Gb/s. The driver for the VCSEL and the receiver for the metal–semiconductor–metal (MSM) detector are also built in the chips. The optoelectronic layer includes 16 × 16 VCSEL–detector arrays, which are flip-chip bonded to the top of the silicon chip stacks. The optics module is a folded hybrid micro-macro imaging system that implements global and regular interconnections. The use of a top concave mirror substantially improves the imaging quality of the optical system and allows a relatively large misalignment tolerance. The system is symmetric, and modular design is used. Commercially available optical components are employed to reduce the cost. The system also possesses features such as high resolution, large field of view, high link efficiency, and low optical cross talk. Scaling of the macrolenses can be used to adjust the interconnection length between the chip stacks. All the optical and optoelectronic components can be packaged with simple passive-alignment technologies. The optics and electronics layers are separated until the final assembly step. The optomechanic module can be snapped onto the electrical system via pins and can be removed and replaced, permitting the system to be reworked.

This paper is organized as follows. Section 2 briefly introduces the system architecture, and Section 3 describes the 3D chip stacks and optoelectronic devices. In Section 4 the design of the optical modular system is presented. Section 5 discusses the system packaging while Section 6 shows some experimental testing results of the system. Finally, a conclusion is given in Section 7.

2. System Concept

Performance of computing systems is becoming increasingly dependent on interconnection networks. The crossbar is one of the most general reconfigurable networks. Each of the nodes in the input stage can be switched to any node in the output stage without blocking. Because it is a single-stage network, latency is minimum compared with that in multiple interconnection networks. However, the number of switching elements increases with N² as the number of nodes N increases. The 2D electronic implementation is costly and complex for large N. Thus such an architecture does not allow good scalability, and the bandwidth of an electronic crossbar is severely limited. To achieve a distributed crossbar, multiple
(L) \( M \times M \) (\( L \times M = N \)) switches are arranged in a multichip module or in a single chip. For various arrangements the total area is of the same order. Many optical crossbar switches have been demonstrated on the basis of free-space\(^{16,31–34} \) or wavelength-division-multiplexing\(^{35} \) technologies. However, only a small number of nodes were handled in some systems. The implementation that uses fan-out optics\(^{31,32} \) suffers from low efficiency in energy utilization, and the point-to-point beam-steering optics\(^{16} \) that uses angle multiplexing requires an array of VCSELs for a single data line. Here we present an optoelectronic system that is scalable and can provide a large communication bandwidth by embedding active electronic switches into chip stacks and incorporating free-space optical interconnections.

Figure 1 shows a schematic diagram of the demonstration system in which three 3D VLSI stacks are assembled with optoelectronic modules for global communications. Each stack consists of 16 VLSI chips and a single 16 \( \times \) 16 VCSEL–MSM detector array flip-chip bonded on top of the chip stack. Each chip in the stack supports 16 optical I/Os at 1 Gb/s, which are connected to 64 electronic I/Os at 250 Mb/s through 4 to 1 multiplexer and 1 to 4 demultiplexer. Furthermore, the electronic chip implements a 16 \( \times \) 16 crossbar switch that can arbitrarily route data packets between its inputs and outputs. The electronic switch, transmitter driver, and the detector amplifier are built in the same layer. In each stack the 16 chips are interleaved with diamond layers for heat removal. A corner-bonding technique was developed to attach the stack onto a support board. A flexible cable attached to the side of the stack provides the system electrical address, control, clock, power, and ground lines to the stack. An optical interconnection layer is designed for global communications between neighboring stacks. The chips in the central stack are perpendicular to those in the other two stacks so that a signal in one end stack can be routed to any chip on the opposite end stack. To realize communication with both the left and the right neighbors, the optoelectronic array is separated into two halves, and the beams in the two halves are deflected differently. The crossbar bandwidth is designed to be 256 Gb/s with a 16 Gb/s throughput per chip.

Figure 2 shows the fixed mapping between the two neighbor optoelectronic arrays; the two arrays are interleaved as a single array. The VCSEL and the detector arrays are offset by 250 \( \mu \)m in the transverse directions. The pitch of the VCSEL array and that of the detector array both are 500 \( \mu \)m. For example, an input signal to the port 0 can be switched in the \( x \) direction to any of the 16 output nodes, and then this signal is routed by the optical system to the corresponding detector on the right stack. After the amplification and thresholding operations, this signal is further switched in the \( y \) direction to any of the output positions. Finally, this signal can be transmitted to the next neighbor stack or back to the left stack, depending on the operation mode and output channel (in the right or left half of the stack). In this way, an input signal can be guided in the \( xy \) plane with the active electronic switches and the optical interconnection in the \( z \) dimension, and the 2D data array can be switched in parallel. The system is easier to scale and can achieve a bandwidth much higher than the all-electronic system. The use of chip stacks greatly reduces the footprint area in comparison with the 2D implementation.

3. Three-Dimensional Chip Stacks and Optoelectronic Array Devices

Three-dimensional stacking of VLSI chips with interleaved diamond heat-spreading layers and integration of the optoelectronic array onto the chip stacks
are challenging. When the design of the buffer chip, including the driver and receiver circuits, was finalized, a buffer prototype cube with a bump-bonded active VCSEL–detector array was designed for investigating the optoelectronic array integration and for the testing and understanding of alignment and packaging issues on chip stacks. Irvine Sensors Corporation stacked the chips in a 3D fashion to form a cubic device, and Honeywell Technology Center fabricated the optoelectronic array and integrated the array with the cube by a flip-chip bonding technique. The I/H2O862O side of the cubes has AlN-based ceramic interface with Au traces. The optoelectronic array side has pads with TiWCuAu metalization to allow flip-chip bonding. Figure 3/H20849a shows the emulator cube with the optoelectronic array. A new attachment process was developed to allow interface with an external test board by use of a flexible cable attached to buffer stacks. The process consists of attaching a flexible cable onto the top cap chip and wire bonding the pads between parts. The opposite end of the flexible cable is designed to fit in a standard connector and thus can be mounted to a board for testing. Figure 3(b) shows the top view of the prototype cube with five VCSELs at the upper left corner switched on. The light intensity versus current (L–I) curve of the VCSEL working at 850 nm is depicted in Fig. 3(c). The threshold current and the threshold voltage are approximately 1.3 mA and 2.0 V, respectively. The VCSEL has an aperture of 5 \( \mu \text{m} \) with a full divergent angle of 30°, and the detector is a 50–\( \mu \text{m} \) octagon.

Figure 4(a) shows one of the new cubes to be used in our system. The size of the cube is 14 mm \( \times \) 14 mm \( \times \) 8 mm. The threshold current and the threshold voltage of the VCSEL are 0.45 mA and 1.65 mV, respectively, with a slope efficiency of 0.4 W/A, and the devices operate at 1 Gb/s. The VCSEL can work over a large temperature range. The responsivity of the detector at 850 nm is 0.25 A/W at 5 V (0.2 A/W at 2 V). All the electrical I/Os are rerouted to the center of the top and bottom surfaces of the cube, and power and control lines are rerouted to the edges of the two surfaces. On the top surface [Fig. 4(b)], there are 1024 pads with TiW Ni Au metalization. (Each I/O channel has four pads: two for the VCSEL and two for the detector. Each chip has 64 pads). The solder dam opening is 40 \( \mu \text{m} \). On the bottom surface [Fig. 4(c)], there are 64 \( \times \) 16 pads with a pitch of 110 \( \mu \text{m} \times 250 \mu \text{m} \), and these pads can be used as the electrical I/Os. The cube is attached to the rigid section of the flexible cable with the corner-bonding technique, which is based on forming a bump at the corner of the cube to the substrate. There is an opening at the center of the rigid section of the flexible cable so that the backside of the cube can be probed. Figure 4(d) shows some VCSELs working at the threshold current.

### 4. Optical Design

Owing to the small feature sizes of the VCSELs and detectors and the relatively large device array, stringent requirements are placed on the optical imaging system. The general requirements on the free-space optical systems are high resolution (small spot size), low loss (high link efficiency), low cross talk, large field of view, low cost, small volume, large misalignment tolerance, simple and cascadable (modular design). Four types of free-space optical systems have been proposed for parallel optical array interconnection: macro-optics with conventional compound lenses,\textsuperscript{10–14} micro-optics with a lens array,\textsuperscript{9,15} hybrid

---

**Fig. 2.** Mapping between two neighbor VCSEL–MSM detector arrays.
optics that uses a microlens array and simple macro lenses,16–20 and mini-optics with a minilens array or minihybrid lenses.21 Generally speaking, the hybrid optical system is optimal in realizing the goals. If the VCSEL–detector arrays are coplanar, the optical system should be folded with a reflection mirror. Here a novel hybrid micro–macro-optical system that satisfies the above requirements is designed, with a concave reflection mirror, and the methodology can be extended to other similar applications.

The optical module that interconnects the two neighboring stacks is shown in Fig. 5. The system is a combination of a pair of small field, low $f$-number microlenses, a pair of large field, high $f$-number macro lenses, a pair of deflecting elements (prisms or gratings), and a concave reflection mirror. In this system the microlens array is used to collimate the beams emitting from the VCSELs and refocus the beams onto the detectors. The macro lenses are used to adjust the interconnection distance. Both the microlens and macro lens are used at infinite conjugates, and the beams are focused at the common focal plane of the two macro lenses. A high resolution is provided by the microlenses, and the macro lenses need to resolve only the aperture of the microlenses. Hence the performance requirements on the macro lenses are greatly reduced. This system combines most of the strengths of the macro- and micro-optical configurations. It is more suitable for the imaging of large dilute arrays with a field larger than that in conventional macro-optical imaging, and it does not suffer from the cross-talk limitations on the interconnection length for purely micro-optical imaging. Infinite conjugate systems are easier to align and tend to increase the tolerance to mechanical misalignment. The deflecting elements are inserted in the collimated beam path between the micro- and macro lenses so that they do not generate additional aberrations. Because the aberrations of an imaging

Fig. 3. Prototype cubic device by integration of a silicon chip stack and a VCSEL–MSM detector array. (a) 3D view. A flexible cable is wire bonded onto the top cap chip. (b) Top view of the optoelectronic array with five VCSELs on. (c) L–I curve of one VCSEL.
system increase with increasing numerical aperture, it is helpful to use a large $f$-number macrolens to improve the imaging quality. The microlens should be chosen to match the VCSEL beam property so that there is no beam clipping at the aperture of the microlens. However, in this configuration the small $f$-number microlenses have severe mechanical tolerance constraints. A small alignment error of the microlens may greatly deteriorate the images. To compensate for the aberrations caused by the misalignment of the microlens and other optical elements, instead of the use of a flat reflection mirror, a concave reflection mirror whose radius is close to the focal length of the macrolens was employed. Further, to reduce the cost, the macrolenses and the concave mirror were selected from off-the-shelf components. The macrolens (KPX088) with a $f/2.9$ and the concave mirror (KPC031, with reflection coating on the concave side) were purchased from Newport Corp. For the beam-deflecting elements, both prisms and diffraction gratings have been considered in different
systems. Although the use of blazing gratings make a more compact system, the loss of energy in the system could be higher than when prisms are used because fabrication errors affect the diffraction efficiency. In particular, in our case, the beams emitting from the left and the right parts of the VCSEL array are deflected to different and symmetric directions, and diffraction of the gratings to the undesired orders will generate communication cross talk. In the prism approach, if the two prisms with knife edges on the sharply acute angle of 21.8° are placed as shown in Fig. 6, two columns of the optical I/O channels might be lost because the bevel width of the edges is comparable with the pitch of the VCSEL–detector array. To overcome this problem, we would rather have a flat of 0.5 mm and have no bevel [Fig. 6(b)]. Then the two prisms are butted up so that the 0.5 mm × 15 mm faces touch [Fig. 6(c)]. The burden was transferred from the bevel to chipping.

By adjustment of the vertical position of the concave mirror, the system can tolerate a significant misalignment of the microlens. The simulation results with CODE V are listed in Table 1. For more accurate modeling, the object is considered as an extended source that encompasses a diameter set to contain 99% of the energy of the Gaussian beam. For example, when the mirror is put at the reference position, the image spot size is less than 4.8 μm in diameter. Even if the microlens is deviated +30 to −30 μm from the reference position, more than 95% of the energy can be encircled in spots no bigger than 14.2 and 25.0 μm, in diameter, respectively. When the VCSEL–detector array is outside the focal plane of the microlens, i.e., the beam coming out of the microlens is convergent, the system has better optical performance than when the VCSEL–detector array is inside the focal plane of the microlens (the beam leaving the microlens is divergent). Moreover, image shift that is due to the lateral alignment error of the cubes can also be compensated for by adjustment of the top mirror. These features permit the cost of packaging to be reduced.

A comparison between use of a concave mirror and use of a plane mirror can be made in terms of the encircled energy versus the spot size. CODE V modeling is shown in Fig. 7, in which ray tracing for three different fields of the object plane is performed. Field 1 is located on axis, field 2 and field 3 are at the edge, and the outmost corner is as shown in Fig. 2. For the Newport macrolens, mentioned above, if the plane mirror is put at the reference position, 50% of the energy is encircled in a spot approximately 11 μm in diameter while 60% of the energy is encircled in a spot approximately 200 μm in diameter. This efficiency and image quality might not be good enough for high-speed interconnection. The modeling shows that to guarantee high image quality, the use of a plane mirror requires a specially designed macrolens and the tolerance for the misalignment of the microlens is quite small. Thus the use of a concave mirror has significant advantages.

The optical system we utilized is scalable. The larger f-number macrolens is more suitable for applications in which the optoelectronic arrays are

<table>
<thead>
<tr>
<th>Longitudinal Misalignment of the Microlens (μm)</th>
<th>Vertical Adjustment of the Top Mirror (mm)</th>
<th>Encircled Energy (%)</th>
<th>Spot Diameter (μm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>30</td>
<td>0</td>
<td>95</td>
<td>14.2</td>
</tr>
<tr>
<td>20</td>
<td>0</td>
<td>100</td>
<td>13.0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>100</td>
<td>4.8</td>
</tr>
<tr>
<td>−20</td>
<td>10.8</td>
<td>85</td>
<td>20.0</td>
</tr>
<tr>
<td>−30</td>
<td>10.8</td>
<td>95</td>
<td>25.0</td>
</tr>
</tbody>
</table>
sparsely distributed. In our demonstration system the chip stacks are put as close as possible to each other to show the functional density. It is possible to design lower f-number macrolenses and choose the corresponding concave reflection mirror. This system will be even more compact.

5. System Packaging

The whole system includes three layers: the system printed circuit board, the optoelectronic module including the three cubes with the VCSEL–detector array and the microlens array, and the optics module. The optoelectronic module and the optics module are assembled separately. The two modules can be removed from the system printed circuit board and replaced, and the optical module can also be removed from the optoelectronic module and replaced.

Before the cubes are assembled in the system, the microlens array is integrated on top of the VCSEL–detector array on the basis of a telecentric imaging system. Both the microlens array and the VCSEL–detector array have a substrate, and the two substrates are integrated together with an adhesive. To align the three cubes into the system, a single aluminum plate and a photomask with registration marks for each other are fabricated. The aluminum plate (MIC 6 Tool Plate, by Euramax Coated Products Ltd.) is used to hold the cubes with better heat dissipation and a more rigid structure. Figure 8(a) is a top view of the aluminum plate. There are three square openings and some alignment crosses on the plate. At the bottom of the photomask [Fig. 8(b)], there are matched alignment crosses and alignment marks registered to the three microlens arrays. The alignment marks for the microlens array are designed in such a way that the distance between the two neighbor lines is equal to the diameter of the microlens. A microscope mounted on a three-axis translation stage is used for accurate alignment. The photomask is first aligned on the aluminum plate and fixed with Kant-Twist clamps. The cubes are aligned one by one. Figure 9 is a picture of the setup. The profile of the cube after assembly is shown in Fig. 10. A thin aluminum plate (part 4) is attached to the bottom of each cube (part 3), then it is fixed to the center of the top surface of a three-axis translation and three-axis rotation stage, with a glue that can be released by a corresponding solvent. The edge of the top surface of the chip stack is held against the machined shoulder at the opening squares of the aluminum plate. The surface of the shoulder is kept parallel to the top surface of the aluminum plate. By adjusting the stage, the cube

![Fig. 7. Comparison between the use of a concave mirror and the use of a flat mirror in terms of the spot size at the detector plane. Simulation results are shown in (a) for the concave mirror and (b) for the flat mirror.](image1)

![Fig. 8. Alignment marks on (a) the aluminum plate and (b) the photomask.](image2)
will be well positioned when the microlens array is matched to the alignment marks on the photomask. To fix the cube with the main aluminum plate (part 1), a small aluminum cube (part 5) is attached to both sides of the thin aluminum plate (part 4), and then the two aluminum plates (parts 1 and 5) are connected with each other with a piece of glass (part 6) and UV-cured epoxy. As shown in Fig. 10, the prisms and the macrolens are assembled into the frame of a single piece of a plastic module. Sufficient alignment precision can be guaranteed by the mechanic fabrication. Each top concave mirror is aligned with a separate plastic piece with screws and springs for adjustment of translation in the vertical direction and tilt along the transverse axes. The optics module and the optoelectronics layer are assembled together with the pin–pinhole technique. They are self-aligned, and no further adjustment is required. Finally, the whole optomechanics module is assembled to the system board by a conventional mechanic method. These modules can also be mounted by use of LEGO.24 Figure 11 is the picture of the optoelectronic system. In the whole packaging procedure, only passive alignment is required, and all the components are easy to align.

Each step of the assembly might generate misalignment. The lateral and rotational misalignments in the system may result in beam coupling in adjacent channels, and the longitudinal misalignments may result in beam clipping at the apertures and defocusing at the detector. Performance simulation of the optical system after assembly can be carried out in CODE V by taking into account all the possible alignment errors. The aluminum plate holding the cubes can be used as a reference plane. Table 2 lists some typical misalignment errors of various components, and the VCSEL–detector array is assumed to be outside the focal plane of the microlens. The image spot diagram for five different fields is shown in Fig. 12. It can be seen that 90% of the energy is encircled in a spot smaller than 12.4 μm in diameter. Table 3 lists various misalignment errors of the VCSEL–detector array and the top mirror while the other errors are kept the same as in Table 2. The VCSEL–detector array is assumed to be inside the focal plane of the microlens. The image spot diagram is shown in Fig. 13, and 90% of the energy is encircled in a spot smaller than 22.9 μm in diameter. Therefore, after considering the misalignment errors of the optical components, the optical system can still

<table>
<thead>
<tr>
<th>Component</th>
<th>Δx (μm)</th>
<th>Δy (μm)</th>
<th>Δz (μm)</th>
<th>α (rad)</th>
<th>β (rad)</th>
<th>γ (rad)</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCSEL</td>
<td>1</td>
<td>1</td>
<td>20 μm</td>
<td>0.008</td>
<td>0.008</td>
<td>0.001</td>
</tr>
<tr>
<td>Prism</td>
<td></td>
<td></td>
<td></td>
<td>0.008</td>
<td>0.008</td>
<td>0.001</td>
</tr>
<tr>
<td>Mirror</td>
<td>5</td>
<td>5</td>
<td>1 mm</td>
<td>−0.01</td>
<td>0.01</td>
<td></td>
</tr>
<tr>
<td>Prism</td>
<td></td>
<td></td>
<td></td>
<td>0.008</td>
<td>0.008</td>
<td>0.001</td>
</tr>
<tr>
<td>Detector</td>
<td>1</td>
<td>1</td>
<td>20 μm</td>
<td>0.008</td>
<td>0.008</td>
<td>0.001</td>
</tr>
</tbody>
</table>

aThe VCSEL–detector array is assumed to be aligned outside the focal plane of the microlens array.

Fig. 9. Cube alignment setup.

Fig. 10. Optomechanic module. 1, main aluminum plate; 2, chip stack; 3, rigid part of the flexible cable; 4, thin aluminum plate; 5, aluminum cube; 6, glass; 7, UV-cured epoxy.

Fig. 11. Assembled optoelectronic system.

Fig. 12. Image spot diagram for five different fields.
satisfy the link requirement well. In the whole packaging procedure, only passive alignment is required, and all the components are easy to align.

6. Experimental Results
In the preliminary experiment, we tested the alignment tolerance of the optical components. Characterization of the optical link at high speed is being investigated, and the results will be presented in future publications. As shown in the previous sections, the top concave mirror can compensate for the optical aberrations and significantly improve the optical performance. When all the optical components are assembled in the system, the top mirror is the only element that can be adjusted, and its alignment has an important effect on types of interconnection performance such as link efficiency and cross talk. In the experiment the top mirror is mounted on a six-axis stage so that it can be moved in the $x$, $y$, and $z$ directions and tilted along the $x$ and $y$ axes. Figure 14 shows the output signal from the MSM detector when the data rate is 2 K/s. To measure the link efficiency, a single VCSEL is switched on. The top mirror is adjusted to find the maximum power incident on the corresponding detector, which is obtained by the photocurrent and the responsivity of the detector. The output power of the VCSEL should be measured before the microlens is integrated. The link efficiency of the optical system is higher than 85%, which is good enough for the receiver at high-speed operation. Cross talk is measured by testing the photocurrent from the neighbor detectors of the desired destination. The responses from the detectors that are located at different distances from the destination are almost the same. This indicates that the cross talk is not caused by the optical system.
Fig. 15. Experimental results for the top mirror tolerance. (a) Tolerance for lateral shift in the $x$ direction. (b) Tolerance for lateral shift in the $y$ direction. (c) Tolerance for vertical shift in the $z$ direction. (d) Tolerance for tilt along the $x$ axis. (e) Tolerance for tilt along the $y$ axis.
but by electronics. This is consistent with the result of code V modeling because the spot size is much smaller than the pitch of the detectors. The detected electrical cross talk is approximately $-24$ dB. The dependence of the performance on the alignment of the top concave mirror is depicted in Fig. 15. Figures 15(a) and 15(b) show the normalized link efficiency versus the lateral translation along the $x$ and $y$ axes, respectively. It can be observed that the tolerance for a 10% drop from the maximum link efficiency can be larger than 100 $\mu$m. Figure 15(c) represents the tolerance of the top mirror in the $z$ direction, and the range of displacement corresponding to the 10% drop in link efficiency is much more than 2 mm. The tilt of the top mirror is measured by use of an autocollimator that illuminates a beam to the backside of the mirror. The normalized link efficiencies as the mirror is tilted along the $x$ and $y$ axes are shown in Figs. 15(d) and 15(e), respectively. The tolerance for the 10% drop in link efficiency is more than 7 arc min. In comparison, the optical performance is more sensitive to the tilt than to the translation in the three dimensions. This result also validates our mechanism positioning of the top mirror, which can be adjusted for tilt along the lateral axes and translation in the longitudinal direction. Tilt of the mirror shifts the spot in the detector plane and can be used to compensate for the lateral misalignment of the cubes, whereas translation of the top mirror can be used to compensate for the misalignment of the microlens.

7. Conclusion

In this paper we have presented a compact scalable optoelectronic switching system with a high bandwidth. It combines the advantages of 3D chip stacks in smaller volume and with high-density powerful processing capability of silicon and those of optics in global, high-speed parallel interconnections. The demonstrator requires several key technologies, including the monolithic integration of VCSELs and MSM detectors into a single array, 3D stacking of silicon chips, hybrid integration of the optoelectronic device array with the silicon chip stacks, optical system design, and system packaging. For the free-space optical interconnection, a novel folded hybrid micro–macro optical system has been designed. The system can provide a high resolution, a large field of view, a high link efficiency, and low optical cross talk. The system is also symmetric and modular. Off-the-shelf macro-optical components are used. By employment of a concave reflection mirror, the image quality can be significantly improved, and it tolerates a large misalignment of the microlens array. The top mirror can also compensate for the lateral shift of the chip stacks. The scaling of the macro lens can be used to adjust the interconnection length between the chip stacks or make the system more compact. The components are easy to align, and only passive alignment is required. We show that by using commercially available optical components and simple passive packaging techniques, it is possible to achieve a high-performance optical interconnection system. An optoelectronic device array with a high density or larger footprint area can be utilized and, correspondingly, the optical system can be redesigned. Our future research includes characterization of the high-speed optical link and switching function.

The authors thank Mark M. Wang, Christoph Berger, and Xuezhe Zheng for helpful discussions. This effort is sponsored by the Defense Advanced Research Projects Agency and the U.S. Air Force Research Laboratory under agreement number F30602-97-2-0122.

References


